A 60 GHz wide band Direct Downconversion Receiver in 40 nm CMOS

Nico De Clercq, Wim Dehaene and Patrick Reynaert
Katholieke Universiteit Leuven, Dept. Elektrotechniek, afd. ESAT-MICAS
Kasteelpark Arenberg 10, B-3001 Heverlee, Belgium
Email: nico.declercq@esat.kuleuven.be

***Abstract*—A 60 GHz receiver front-end with 6 GHz RF bandwidth and 4 GHz baseband bandwidth is presented. The chip consists of an LNA and quadrature direct downconversion mixers, directly connected to a high impedant digital baseband. An on-chip poly-phase filter is used to generate the necessary quadrature LO signals from an external reference. A fully differential architecture is used to alleviate the influences of parasitics and avoid common-mode stability problems. A test chip was fabricated in a 1P10M $40\,\mathrm{nm}$ CMOS process. A noise figure of $10.8\,\mathrm{dB}$ and input P_{1dB} of $-9\,\mathrm{dBm}$ were measured. The front-end has a power consumption of $80\,\mathrm{mW}$ from a $1.1\,\mathrm{V}$ supply.**

I. Introduction

The large unlicensed frequency spectrum around 60 GHz, has recently gained a lot of attention. The available bandwidth of about 7 GHz, combined with a high allowed transmitted power level, provides an excellent opportunity for numerous applications. These applications include short range multi-Gb/s wireless communication systems [1], mm-range wireless ranging applications [2], ...High data rates are desirable in numerous applications, like Wireless Personal Area Networks (WPAN), wireless HDMI and wireless docking stations [1]. The high-volume consumer market could be adressed with the availability of fully integrated mm-wave technology. Only recently innovations in manufacturing have made the use of these mm-wave frequencies possible in standard CMOS technology, as can be seen by the amout of recent publications. The use of CMOS technology is crucial to achieve a cost effective solution in high volume applications.

In this paper a 60 GHz receiver front-end, with 6 GHz RF bandwidth and 4 GHz baseband bandwidth is presented. The receiver was implemented in a 1P10M $40\,\mathrm{nm}$ CMOS technology. The circuit interfaces with an on-chip digital baseband, expected to be implemented on the same die. First the fully-differential receiver architecture is discussed. Afterwards the design of the LNA and mixer circuits is addressed. The quadrature clock signal generation, from an external 60 GHz clock, is presented in section 4. The final section summarizes the measurement results of the fabricated test chip.

II. Receiver Architecture

The zero-IF receiver architecture consists of a fully differential LNA followed by a quadrature downconversion stage, as shown in figure 1. The I/Q LO signals needed to drive the mixers are generated by means of an on-chip poly-phase filter (PPF) driven from an external 60 GHz source. Buffers are needed to compensate for the high insertion loss caused by the PPF. The downconverted signals are applied directly to the digital baseband circuit. Bondpads are connected to the I/Q baseband to allow the RF front-end to be characterized separately.

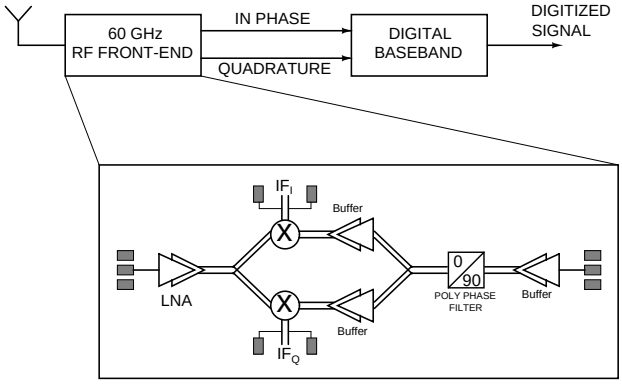


Fig. 1. 60 GHz Receiver architecture

III. LNA Design

The schematic of the fully differential LNA is shown in figure 2. A two stage topology is used to achieve a higher gain. At the input a transformer performs the single-ended to differential conversion. Transformers are also used to couple both stages and to couple the second LNA stage to the down-conversion mixers. The use of transformer coupling allows wideband matching and is convenient to easily provide the DC bias of the transistors. The use of series capacitive coupling, typically used in DC biasing structures, would result in a higher loss due to lower capacitive Q factors at 60 GHz. Slow wave transmission lines (SWTL) are placed in series with the transformers, to achieve a broad band impedance match.

For the design of the LNA stages, the bias current density was chosen first and set to the NF_{min} current density of approximately $150\,\mathrm{uA/um}$ [3]. Afterwards the transistor finger width is chosen, to maximize f_{max} and simultaneously minimize NF_{min}. The optimal source impedance (Z_S) can now be determined by plotting the constant noise and the available gain circles on a smith chart. Gain can be traded for noise, depending on the position of Z_S on the smith chart with respect to the optimal noise and gain points. Once Z_S is

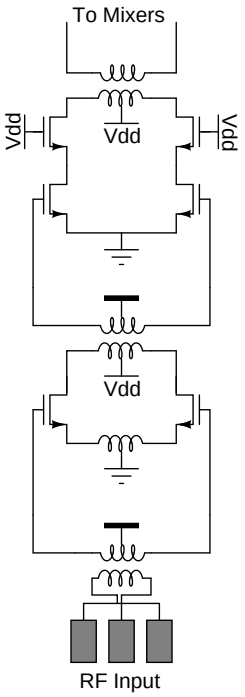


Fig. 2. Schematic of the fully differential LNA

chosen, the load impedance of the stage is chosen to achieve conjugate matching.

The 60 GHz input signal is applied by means of a GSG RF probe, requiring the input impedance of the LNA to be matched to $50\,\Omega$. At first, a comparisson between a common-source and a cascode topology was performed. A common-source input stage was used, as a cascode stage would result in a higher noise figure. The cascode topology also showed to have a more difficult to match range of source impedances.

$$Z_{in} = \frac{L_s \cdot g_m}{C_{gs}} + \frac{j \cdot \omega \cdot (L_g + L_s)}{j \cdot \omega \cdot C_{gs}} \qquad (1)$$

Furthermore, the input impedance (Z_{in}) of the LNA is dependant on the gate-source capacitance of the input transistor (C_{gs}) and on the inductance at the gate (L_g) and source (L_s) of this transistor (1) . Equation (1) shows that the real part of Z_{in} can be increased by increasing the inductance L_s at the source of the input transistor. In this design inductive source degeneration, of about $50\,\mathrm{pH}$ per transistor, was therefore used in the first stage to achieve a better input match. Simulations show that the degenerating inductor also leads to a reduction of the gain of the input stage. The use of an antenna, with an easier to match input impedance, would ease the design of the passive components and therefore lead to a higher gain.

The difficult to match optimal input impedance of a cascode stage does not pose a problem for the second stage. The output impedance of the first stage is easier to match. A cascode transistor was therefore used in the second stage to achieve a higher gain and a better input-output isolation. Furthermore, a higher noise figure can be tolerated in this stage.

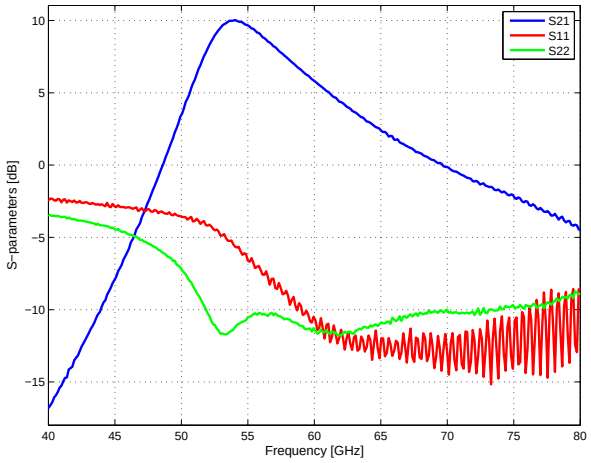


Fig. 3. LNA S-parameter Measurement

A standalone version of the LNA was processed on the same die. This LNA is identical to the circuit used in the receiver, but with the output of the second stage connected to a GSG probe pad. An appropriate matching structure, consisting of SWTL's and a differential to single-ended balun, is used to match the LNA output impedance to the impedance of the measurement equipment. Figure 3 shows the S-parameter measurments of the LNA. The standalone LNA has a gain of about $10\,\mathrm{dB}$, a bandwidth of $7.15\,\mathrm{GHz}$ and a NF of $6.7\,\mathrm{dB}$. It consumes $20\,\mathrm{mW}$ of power.

IV. Mixer Design

The architecture of the downconversion mixers is shown in figure 4. A double balanced topology is used to achieve a better port to port isolation and higher suppression of spurious mixing products. Due to the limited supply voltage, a topology without a transconductance stage was chosen to improve linearity [4]. The RF input signal is supplied directly to the source of the switching transistors by means of $110\,\mathrm{fF}$ series coupling capacitors (C_{cpl}). C_{cpl} has the additional benefit of suppressing the low frequency second order intermodulation distortions from the previous stage. Due to the absence of a transconductance stage, the mixer has a simulated insertion loss of about 3 dB. The IF output connects directly to the digital baseband and the bondpads, needed to characterize the front-end separately. The use of a baseband buffer, able to drive the $50\,\Omega$ load of the measurement equipment, would increase the capacitive load of the mixer. This would lead to an unacceptable decrease of the IF bandwidth.

V. Quadrature LO generation

The quadrature LO signals are generated from an external 60 GHz signal, by means of an on-chip poly-phase filter (PPF). A cascade of 2 PPF stages, one tuned to 58 GHz and the other tuned to 64 GHz, is used to achieve a good image rejection ratio across a wide band of 53 to 67 GHz. The 2 stage topology also increases the robustness against process variations. The structure of the PPF makes a symmetrical layout very difficult,

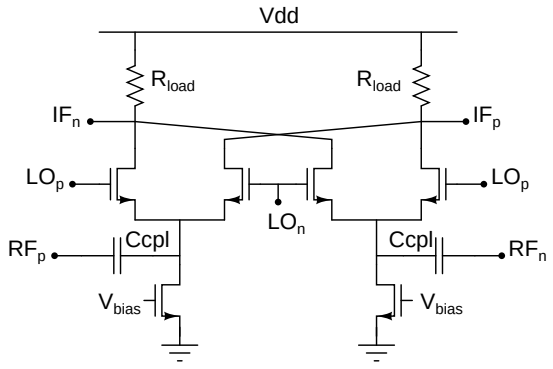


Fig. 4. Direct downconversion mixer

which leads to an unavoidable shift in filter frequency. This effect is overcome by fine tuning the capacitor and resistor values after EM simulations and parasitic extraction.

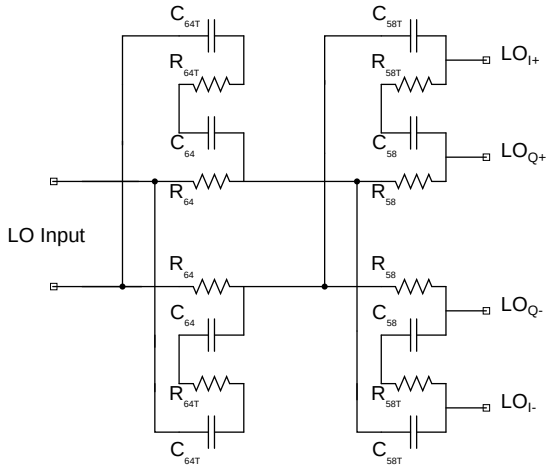
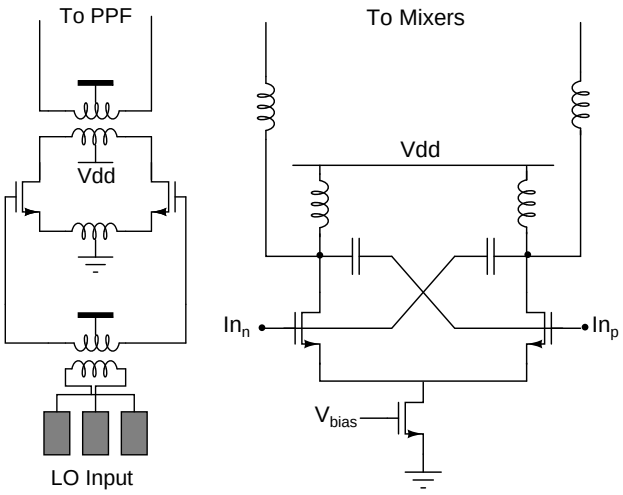


Fig. 5. Two stage Poly Phase Filter used for I/Q LO generation

The PPF results in a high insertion loss. Therefore 60 GHz buffers are added before and after the I/Q generation (figure 6). The second buffer stage (figure 6(b)), at the mixer side, employs capacitive gate-drain neutralization to achieve a higher gain and increase the buffer stability. About $12\,\mathrm{fF}$ of feedback capacitance is used. Series inductors are added between the buffer outputs and the mixers to improve the impedance match. Each mixer side buffer has a power consumption of $10\,\mathrm{mW}$ and a gain of about $10\,\mathrm{dB}$. At the LO input side inductive source degeneration is employed to obtain a good impedance match with the $50\,\Omega$ input probe (figure 6(a)). The input buffer has a gain of about $6\,\mathrm{dB}$ and consumes about $7\,\mathrm{mW}$ of power.

VI. Measurement Results

The circuit was fabricated in a $40\,\mathrm{nm}$ CMOS technology (figure 7). The receiver front-end has a total area of $0.66\,\mathrm{mm}^2$. The standalone LNA consumes $0.25\,\mathrm{mm}^2$ of area. For measurements the chip is mounted on a PCB. Bondwires are used to apply the required DC biasing and connect the IF outputs. The losses attributed to the bondwires and transmission lines



(a) Input PPF buffer (b) Second PPF buffer stage

Fig. 6. Schematics of the PPF Buffers

of the IF output were de-embedded through measurements on a separate PCB containing the same transmission line structures back to back. The mm-wave input and LO signal are applied by on-chip probing. The losses attributed to the mm-Wave probes, cables and connectors were de-embedded from the measurement results.

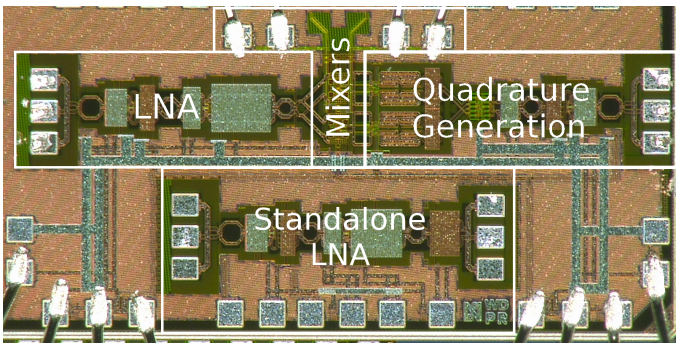


Fig. 7. Chip microphotograph (Receiver $0.66\,\mathrm{mm}^2$, LNA $0.25\,\mathrm{mm}^2$)

The entire RX circuitry consumes $80\,\mathrm{mW}$ of power from a $1.1\,\mathrm{V}$ supply. Figure 8 shows the measured insertion loss and noise figure (NF) versus RF frequency. It has a minimal insertion loss of $8.8\,\mathrm{dB}$ at 55 GHz and a 3 dB RF bandwidth of 6 GHz centered around 56 GHz. The shift in center frequency is attributed to process variations and modelling imperfections. The front-end achieves the 6 GHz RF bandwidth, available in the unlicensed frequency band around 60 GHz. The double sideband noise figure was measured using the direct noise figure measurement method at an IF frequency of 200 MHz. The noise figure, including LNA and mixers, has a minimum of $10.8\,\mathrm{dB}$ at 56 GHz.

The measured insertion loss versus IF frequency is shown in figure 9. The front-end has a high IF bandwidth of 4 GHz. It has a measured input referred 1 dB compression point (P_{1dB}) of $-9\,\mathrm{dBm}$.

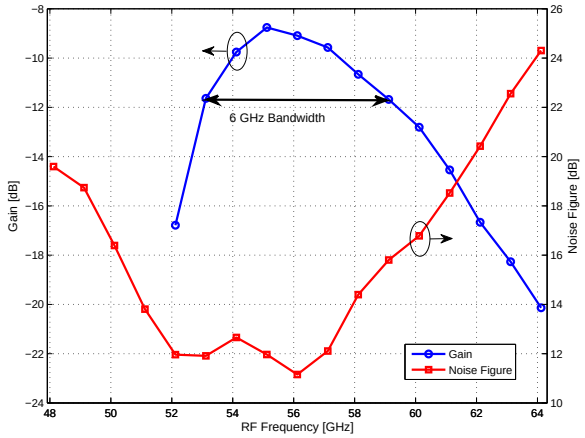


Fig. 8. RF Bandwidth and DSB noise figure (NF) (200 MHz IF frequency)

	This Work	*[5] [ISSCC'12]*	*[6] [ISSCC'12]*	*[7] [ISSCC'11]*
Building Blocks	LNA + I/Q Mixers	LNA + I/Q Mixers + BB Amp.	LNA + Super Het. + BB Amp.	LNA + Super Het. + BB Amp.
Technology	40 nm CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS
Input P_{1dB}	-9 dBm	-31 dBm	NA	-29 dBm
NF	10.8 dB	5.5 dB	14 dB	7.6 dB
Input RF Bandwidth	6 GHz	9 GHz	NA	9 GHz
Input IF Bandwidth	4 GHz	0.95 GHz	1.04 GHz	0.9 GHz
Input $P_{dc}(V_{dd})$	80 mW (1.1 V)	35 mW (1.1 V)	233 mW (NA)	74 mW (1.2 V)

TABLE I
COMPARISON WITH RECENTLY PUBLISHED 60GHZ RECEIVERS

Table I shows a comparison with previously reported state of the art 60 GHz receiver chips. It clearly shows this architecture to achieve the highest IF bandwidth of 4 GHz, while having a comparable power consumption. The fairly high insertion loss is caused by the $50\,\Omega$ load of the measurement equipment. Simulations show the mixer to have an insertion loss of only $3\,\mathrm{dB}$ when the front-end directly drives the digital baseband. This is the case in the final system, as the digital baseband is expected to be on the same die and attached directly to the IF output.

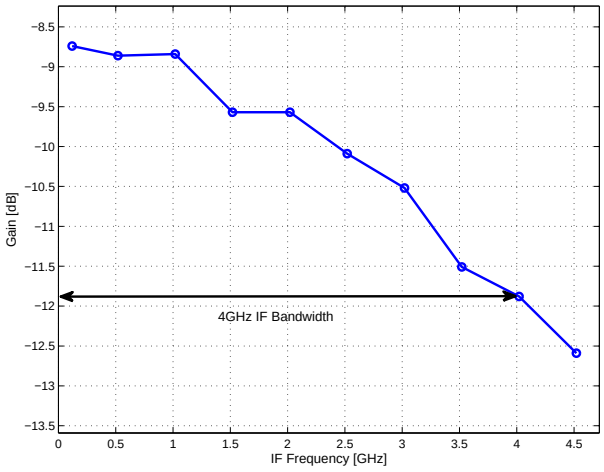


Fig. 9. Measured IF Bandwidth

VII. CONCLUSION

A 60 GHz receiver front-end with a high baseband bandwidth of 4 GHz was presented. A fully differential architecture was used to avoid the influence of circuit parasitics and common-mode stability ptoblems. An LNA and I/Q direct downconversion mixers are included on the test chip, fabricated in a 1P10M $40\,\mathrm{nm}$ CMOS process. A high impedant digital baseband is assumed to be on the same die, and connected directly to the front-end. The quadrature LO signals, needed to drive the mixers, are generated by an on-chip polyphase filter (PPF). Buffers are used to compensate for the high insertion loss of the PPF. A minimal insertion loss of $8.8\,\mathrm{dB}$ was measured, combined with a noise figure of $10.8\,\mathrm{dB}$. The high insertion loss can be attributed to the $50\,\Omega$ input impedance of the measurement equipment, as can be seen from simulations. The front-end has a power consumption of $80\,\mathrm{mW}$ from a $1.1\,\mathrm{V}$ supply.

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REFERENCES

[1] S. Pellerano, Y. Palaskas, and K. Soumyanath, "A 64 GHz LNA with 15.5 dB gain and 6.5 dB NF in 90 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 7, pp. 1542–1552, 2008.

[2] T. Ayhan, T. Redant, M. Verhelst, and W. Dehaene, "Towards a Fast and Hardware Efficient sub-mm precision Ranging System," in *IEEE Workshop on Signal Processing Systems (SiPS), 2012*, 2012, pp. 203–208.

[3] T. Yao, M. Gordon, K. Tang, K. Yau, M. Yang, P. Schvan, and S. Voinigescu, "Algorithmic design of CMOS LNA's and PA's for 60-GHz radio," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 5, pp. 1044–1057, 2007.

[4] P. Sakian, R. Mahmoudi, P. van Zeijl, M. Lont, and A. van Roermund, "A 60GHz double-balanced homodyne down-converter in 65nm CMOS process," in *Microwave Integrated Circuits Conference, 2009. EuMIC 2009. European*. IEEE, 2009, pp. 258–261.

[5] V. Vidojkovic, G. Mangraviti, K. Khalaf, V. Szortyka, K. Vaesen, W. Van Thillo, B. Parvais, M. Libois, S. Thijs, J. Long, C. Soens, and P. Wambacq, "A low-power 57-to-66GHz transceiver in 40nm LP CMOS with -17db EVM at 7Gb/s," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 268 –270.

[6] T. Mitomo, Y. Tsutsumi, H. Hoshino, M. Hosoya, T. Wang, Y. Tsubouchi, R. Tachibana, A. Sai, Y. Kobayashi, D. Kurose, T. Ito, K. Ban, T. Tandai, and T. Tomizawa, "A 2Gb/s-throughput CMOS transceiver chipset with in-package antenna for 60GHz short-range wireless communication," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 266 –268.

[7] A. Siligaris, O. Richard, B. Martineau, C. Mounet, F. Chaix, R. Ferragut, C. Dehos, J. Lanteri, L. Dussopt, S. Yamamoto, R. Pilard, P. Busson, A. Cathelin, D. Belot, and P. Vincent, "A 65nm CMOS fully integrated transceiver module for 60GHz wireless HD applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, 2011, pp. 162 –164.